Abstract of the Disclosure:

A pseudo random signal producing circuit includes a generator 110 for generating a first pseudo random signal having a bit width a (a being an integer not smaller than 1), a generator 120 for generating a second pseudo random signal having a bit width b (b being an integer not smaller than 1 and different from a), a matrix calculator 130 for carrying out matrix calculation upon the first and the second pseudo random signals to produce a calculation result signal having a bit width (a*b), an N-bit shift register 200 responsive to the calculation result signal having the bit width (a*b) for producing an output pseudo random signal having a bit width N (N being a divisor of (a*b)), and a frequency-division clock generator 300 for driving a pseudo random data generator 100.